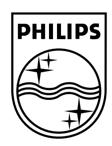
DATA SHEET

TDA8709A
Video analog input interface

Product specification
Supersedes data of April 1993
File under Integrated Circuits, IC02

June 1994

Philips Semiconductors



PHILIPS

Video analog input interface TDA8709A

FEATURES

- 8-bit resolution
- Sampling rate up to 32 MHz
- TTL-compatible digital inputs and outputs
- Internal reference voltage regulator
- Low-level AC clock inputs and outputs
- Clamp function with selection for ‘16’ or ‘128’
- No sample-and-hold circuit required
- Three selectable video inputs.

APPLICATIONS

- Video signal processing
- Digital picture processing
- Frame grabbing.
- Colour difference signals (U, V)
- R, G, B signals
- Chrominance signal (C).

GENERAL DESCRIPTION

The TDA8709A is an analog input interface for video signal processing. It includes a an input selector (one out-of-three video signals), video amplifier with clamp and external gain control, an 8-bit analog-to-digital converter (ADC) with a sampling rate of 32 MHz and an input selector.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage	4.5	5.0	5.5	V
V_{CCD}	digital supply voltage	4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage	4.2	5.0	5.5	V
I_{CCA}	analog supply current	–	40	47	mA
I_{CCD}	digital supply current	–	24	30	mA
I_{CCO}	TTL output supply current	–	12	16	mA
ILE	DC integral linearity error	–	–	±1	LSB
DLE	DC differential linearity error	–	–	±0.5	LSB
$f_{clk(max)}$	maximum clock frequency	30	32	–	MHz
B	maximum –3 dB bandwidth (preamplifier)	12	18	–	MHz
P_{tot}	total power dissipation	–	380	512	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
TDA8709A	28	DIP	plastic	SOT117-1
TDA8709AT	28	SO28L	plastic	SOT136-1

BLOCK DIAGRAM

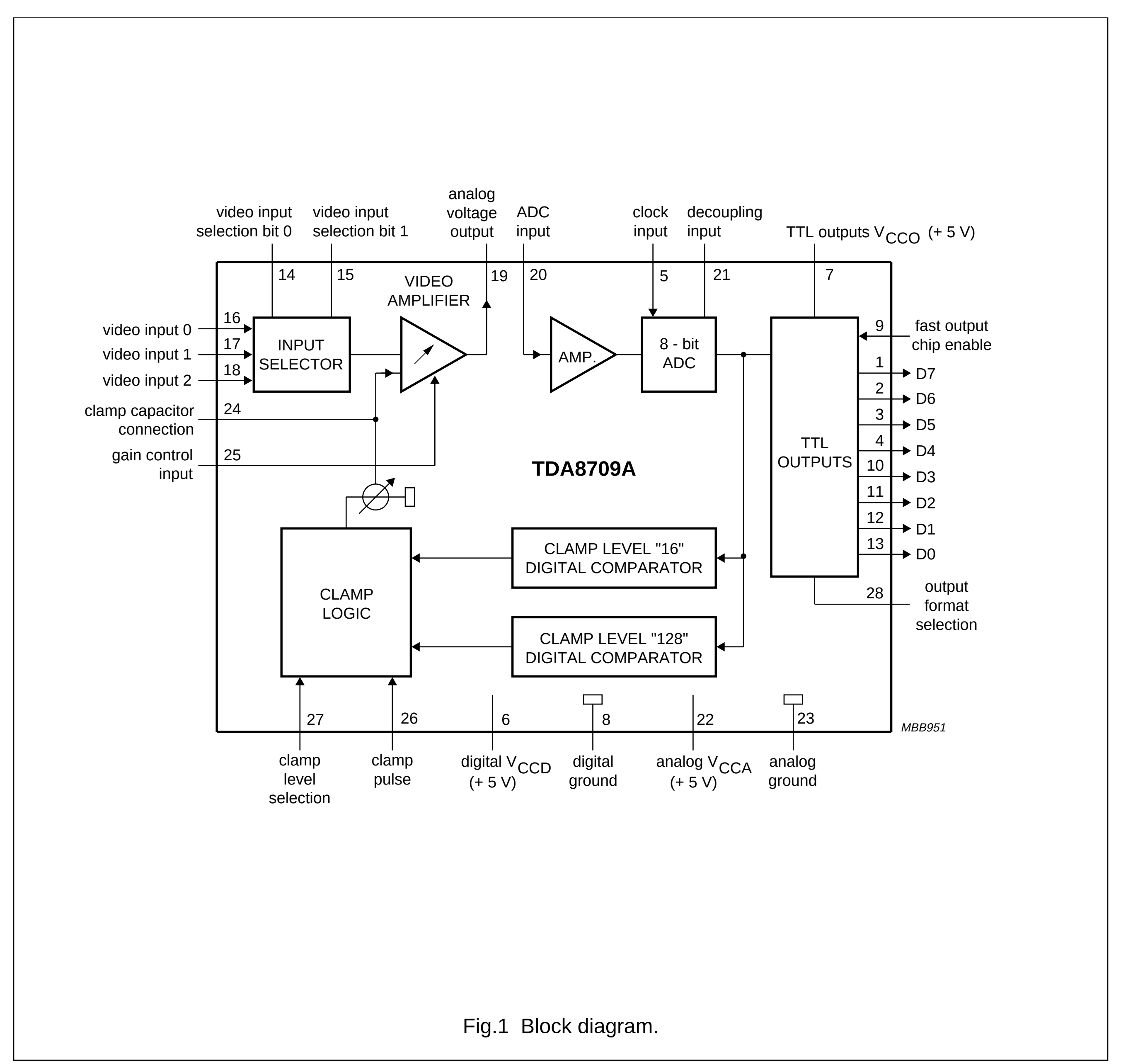


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
D7	1	data output; bit 7 (MSB)
D6	2	data output; bit 6
D5	3	data output; bit 5
D4	4	data output; bit 4
CLK	5	clock input
V_{CCD}	6	digital supply voltage (+5 V)
V_{CCO}	7	TTL outputs supply voltage (+5 V)
DGND	8	digital ground
FOEN	9	fast output chip enable
D3	10	data output; bit 3
D2	11	data output; bit 2
D1	12	data output; bit 1
D0	13	data output; bit 0 (LSB)
I0	14	video input selection bit 0
I1	15	video input selection bit 1
VIN0	16	video input 0
VIN1	17	video input 1
VIN2	18	video input 2
ANOUT	19	analog voltage output
ADCIN	20	analog-to-digital converter input
DEC	21	decoupling input
V_{CCA}	22	analog supply voltage (+5 V)
AGND	23	analog ground
CLAMP	24	clamp capacitor connection
GAIN	25	gain control input
CLP	26	clamping pulse
CLS	27	clamping level selection input
OFS	28	output format selection

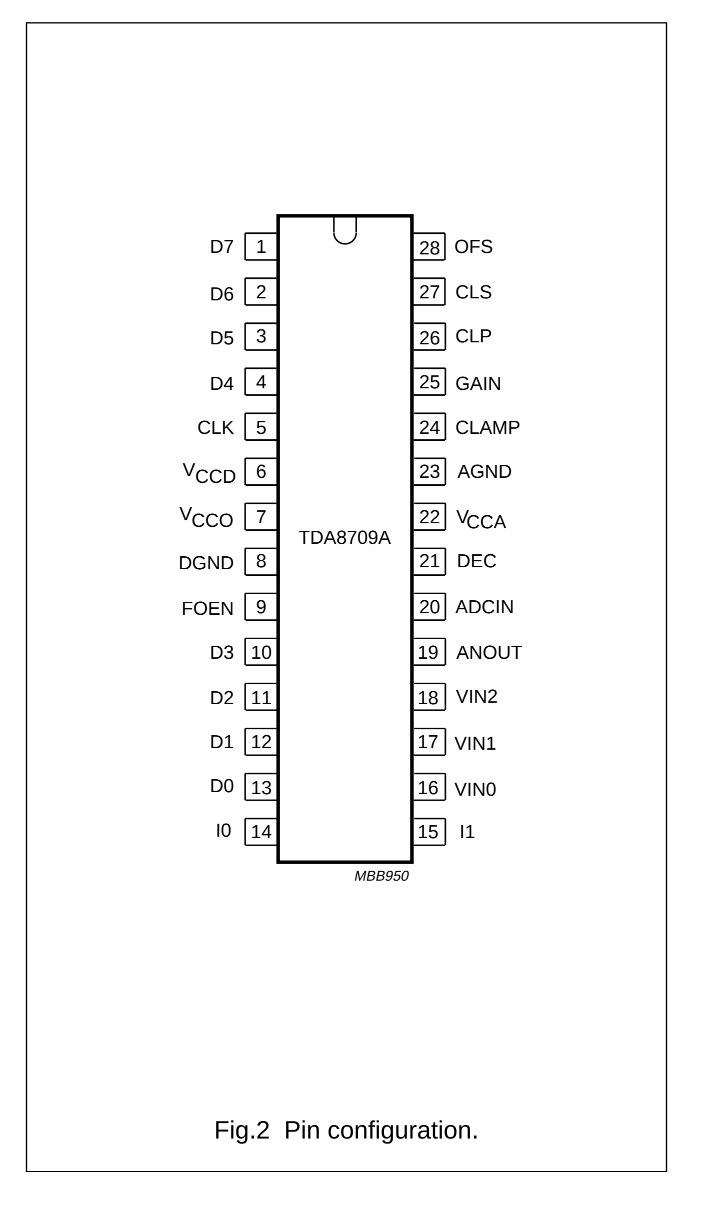


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

TDA8709A is an 8-bit ADC with internal clamping and a preamplifier with adjustable gain.

The clamping value is switched via pin 27 between digital 16 (for R, G, B signals) and digital 128 (for chrominance or colour difference signals). While clamping pulse at pin 27 is logic 1, the device will adjust the clamping level to the chosen value. The output format can be selected between binary and two's complement at pin 28.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	–0.3	+7.0	V
V_{CCD}	digital supply voltage	–0.3	+7.0	V
V_{CCO}	TTL output supply voltage	–0.3	+7.0	V
ΔV_{CC}	supply voltage difference between V_{CCA} and V_{CCD}	–0.5	+0.5	V
	supply voltage difference between V_{CCO} and V_{CCD}	–0.5	+0.5	V
	supply voltage difference between V_{CCA} and V_{CCO}	–1.0	+1.0	V
V_I	input voltage	–0.3	+7.0	V
I_O	output current	–	+10	mA
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	0	+70	°C
T_j	junction temperature	0	+125	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air		
	SOT117-1	55	K/W
	SOT136-1	70	K/W

CHARACTERISTICS

$V_{CCA} = V_{22}$ to V_{23} = 4.5 to 5.5 V; $V_{CCD} = V_6$ to V_8 = 4.5 to 5.5 V; $V_{CCO} = V_7$ to V_8 = 4.2 to 5.5 V; AGND and DGND shorted together; V_{CCA} to V_{CCD} = –0.5 to +0.5 V; V_{CCO} to V_{CCD} = –0.5 to +0.5 V; V_{CCA} to V_{CCO} = –0.5 to +0.5 V; T_{amb} = 0 to +70 °C; typical readings taken at $V_{CCA} = V_{CCD} = V_{CCO}$ = 5 V and T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{CCA}	analog supply voltage		4.5	5.0	5.5	V
V_{CCD}	digital supply voltage		4.5	5.0	5.5	V
V_{CCO}	TTL output supply voltage		4.2	5.0	5.5	V
I_{CCA}	analog supply current		–	40	47	mA
I_{CCD}	digital supply current		–	24	30	mA
I_{CCO}	TTL output supply current	TTL load (see Fig.7)	–	12	16	mA
Preamplifier inputs						
VIN0 TO VIN2 INPUTS						
$V_{I(p-p)}$	input voltage (peak-to-peak value)	note 1	0.6	–	1.5	V
$\|Z_i\|$	input impedance	f_i = 6 MHz	10	20	–	kΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
I0 AND I1 TTL INPUTS (SEE TABLE 1)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
CLS, OFS AND CLP TTL INPUTS (SEE FIG.5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_I = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_I = 2.7 V	–	–	20	µA
t_{CLP}	clamp pulse width		2	–	–	µs
GAIN INPUT (PIN 25)						
$V_{25(min)}$	input voltage for minimum gain	see Fig.9	–	1.8	–	V
$V_{25(max)}$	input voltage for maximum gain	see Fig.9	–	3.8	–	V
I_I	input current		–	1.0	–	µA
CLAMP INPUT (PIN 24)						
V_{24}	clamp voltage for code 128 output		–	3.5	–	V
I_{24}	clamp output current			see Table 2		

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Video amplifier outputs						
ANOUT OUTPUT (PIN 19)						
$V_{19(p\text{-}p)}$	AC output voltage (peak-to-peak value)	V_{OF} = 1.33 V (p-p); V_{25} = 3.0 V	–	1.33	–	V
I_{19}	internal current source	$R_L = \infty$	2.0	2.5	–	mA
$I_{O(p\text{-}p)}$	output current driven by the load	V_{ANOUT} = 1.33 V (p-p); note 2	–	–	1.0	mA
V_{19}	DC output voltage for black level	CLS = logic 1	–	V_{CCA} – 2.02	–	V
V_{19}	DC output voltage for black level	CLS = logic 0	–	V_{CCA} – 2.6	–	V
Z_{19}	output impedance		–	20	–	Ω
Preamplifier dynamic characteristics						
α_{ct}	crosstalk between VIN inputs	V_{CCA} = 4.75 to 5.25 V; note 3	–	–50	–45	dB
G_{diff}	differential gain	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	2	–	%
φ_{diff}	differential phase	V_{VIN} = 1.33 V (p-p); V_{25} = 3.0 V	–	0.8	–	deg
B	–3 dB bandwidth		12	–	–	MHz
S/N	signal-to-noise ratio	note 4	60	–	–	dB
SVRR1	supply voltage ripple rejection	note 5	–	45	–	dB
ΔG	gain range	see Fig.9	–4.5	–	+6.0	dB
G_{stab}	gain stability as a function of supply voltage and temperature	see Fig.9	–	–	5	%
Analog-to-digital converter inputs						
CLK INPUT (PIN 5)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_{clk} = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_{clk} = 2.7 V	–	–	100	µA
$\lvert Z_i \rvert$	input impedance	f_{clk} = 10 MHz	–	4	–	kΩ
C_I	input capacitance	f_{clk} = 10 MHz	–	4.5	–	pF
FOEN INPUT (SEE TABLE 3)						
V_{IL}	LOW level input voltage		0	–	0.8	V
V_{IH}	HIGH level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW level input current	V_9 = 0.4 V	–400	–	–	µA
I_{IH}	HIGH level input current	V_9 = 2.7 V	–	–	20	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ADCIN INPUT (PIN 20; SEE TABLE 4)						
V_{20}	input voltage	digital output = 00	–	V_{CCA} – 2.52	–	V
V_{20}	input voltage	digital output = 255	–	V_{CCA} – 1.52	–	V
$V_{20(p-p)}$	input voltage amplitude (peak-to-peak value)		–	1.0	–	V
I_{20}	input current		–	1.0	10	μA
$\|Z_i\|$	input impedance	f_i = 6 MHz	–	50	–	MΩ
C_I	input capacitance	f_i = 6 MHz	–	1	–	pF
Analog-to-digital converter outputs						
DIGITAL OUTPUTS D0 TO D7						
V_{OL}	LOW level output voltage	I_{OL} = 2 mA	0	–	0.6	V
V_{OH}	HIGH level output voltage	I_{OL} = –0.4 mA	2.4	–	V_{CCD}	V
I_{OZ}	output current in 3-state mode	0.4 V < V_O < V_{CCD}	–20	–	+20	μA
Switching characteristics						
$f_{clk(max)}$	maximum clock input frequency	see Fig.5; note 6	30	32	–	MHz
Analog signal processing (f_{clk} = 32 MHz; see Fig.7)						
G_{diff}	differential gain	V_{20} = 1.0 V (p-p); see Fig.6; note 7	–	2	–	%
φ_{diff}	differential phase	see Fig.6; note 7	–	2	–	deg
f_1	fundamental harmonics (full-scale)	f_i = 4.43 MHz; note 7	–	–	0	dB
f_{all}	harmonics (full-scale); all components	f_i = 4.43 MHz; note 7	–	–55	–	dB
SVRR2	supply voltage ripple rejection	note 8	–	1	5	%/V
Transfer function						
ILE	DC integral linearity error		–	–	±1	LSB
DLE	DC differential linearity error		–	–	±0.5	LSB
ILE	AC integral linearity error	note 9	–	–	±2	LSB
Timing (f_{clk} = 32 MHz; see Figs 5, 6 and 7)						
DIGITAL OUTPUTS (C_L = 15 pF; I_{OL} = 2 mA; R_L = 2 kΩ)						
t_{ds}	sampling delay time		–	2	–	ns
t_h	output hold time		–	8	–	ns
t_d	output delay time		–	16	20	ns
t_{dEZ}	3-state delay time; output enable		–	16	25	ns
t_{dDZ}	3-state delay time; output disable		–	12	25	ns

Notes to the "Characteristics"

1. 0 dB is obtained at the AGC amplifier when applying $V_{i(p-p)}$ = 1.33 V.
2. The output current at pin 19 should not exceed 1 mA. The load impedance R_L should be referenced to V_{CCA} and defined as:
   a) AC impedance ≥1 kΩ and the DC impedance >2.7 kΩ.
   b) The load impedance should be coupled directly to the output of the amplifier so that the DC voltage supplied by the clamp is not disturbed.
3. Input signals with the same amplitude. Gain is adjusted to obtain ANOUT = 1.33 V (p-p).
4. Signal-to-noise ratio measured with 5 MHz bandwidth:

   $$\frac{S}{N} = 20\log\frac{V_{ANOUT\,(p-p)}}{V_{ANOUT\,(RMS\ noise)}}\text{ at B = 5 MHz.}$$

5. The voltage ratio is expressed as:

   $$SVRR1 = 20\log\frac{\Delta V_{CCA}}{V_{CCA}}\times\frac{G}{\Delta G}$$ for V_I = 1 V (p-p), gain at 100 kHz = 1 and 1 V supply variation.

6. It is recommended that the rise and fall times of the clock are ≥2 ns. In addition, a 'good layout' for the digital and analog grounds is recommended.
7. These measurements are realized on analog signals after a digital-to-analog conversion (TDA8702 is used).
8. The supply voltage rejection is the relative variation of the analog signal (full-scale signal at input) for 1 V of supply variation:

   $$SVRR2 = \frac{\Delta\,(V_{I\,(00)} - V_{I\,(FF)}) + (V_{I\,(00)} - V_{I\,(FF)})}{\Delta V_{CCA}}$$

9. Full-scale sine wave (f_i = 4.4 MHz; f_{clk} = 27 MHz).

Table 1 Video input selection (CVBS).

I1	I0	SELECTED INPUT
0	0	VIN0
0	1	VIN1
1	0	VIN2
1	1	VIN1

Table 2 CLAMP output current.

CLS	CLP	DIGITAL OUTPUT	I_{CLAMP}
1	1	output < 128	+50 µA
		output > 128	–50 µA
X[(1)]	0	X	0 µA
0	1	output < 16	+50 µA
		16 < output	–50 µA

Note

1. X = don't care.

Table 3 FOEN input coding.

FOEN	D0 TO D7
0	active, two's complement
1	high impedance

Table 4 Output coding and input voltage (typical values).

STEP	V_{ADCIN}	BINARY OUTPUTS								TWO'S COMPLEMENT							
		D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
Underflow	–	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
0	V_{CCA} – 2.52 V	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	–	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
.	–	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
254	–	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	0
255	V_{CCA} – 1.52 V	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Overflow	–	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

0.25 V
5 MHz sine wave
1.0 V
0.25 V
64 μs
MBB959

Fig.3 Test signal on the ADCIN pin for differential gain and phase measurements.

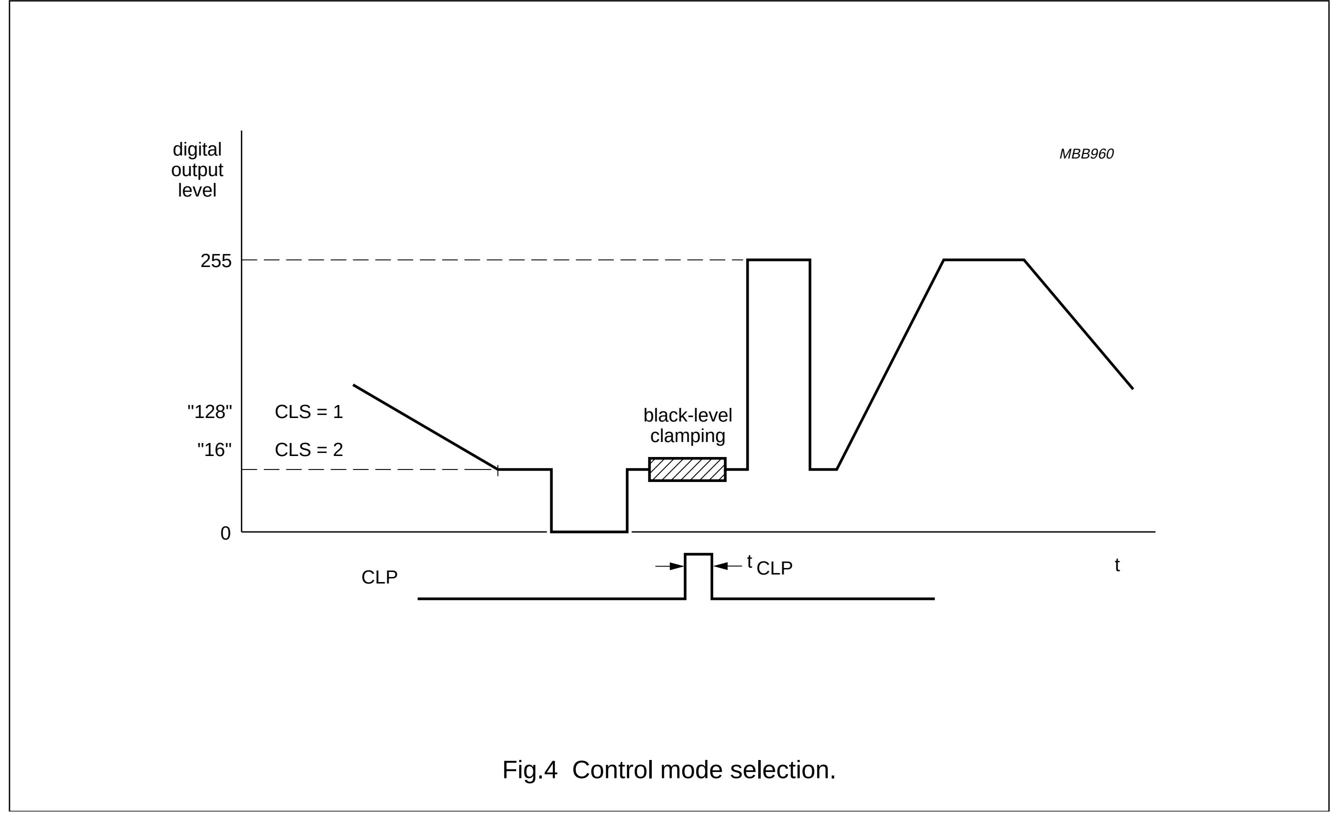


Fig.4 Control mode selection.

Fig.5 Timing diagram.

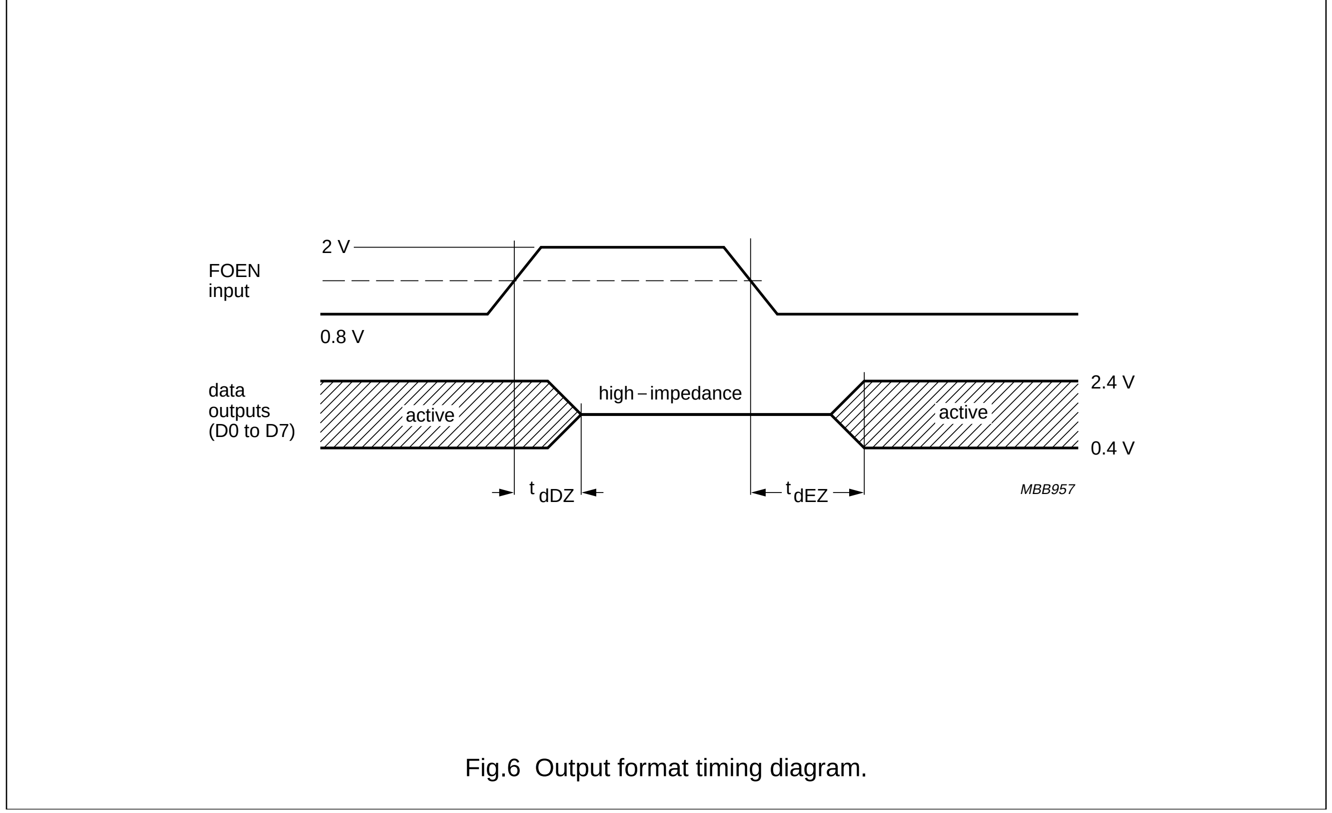


Fig.6 Output format timing diagram.

Fig.7 Load circuit for timing measurement; data outputs (FOEN = LOW).

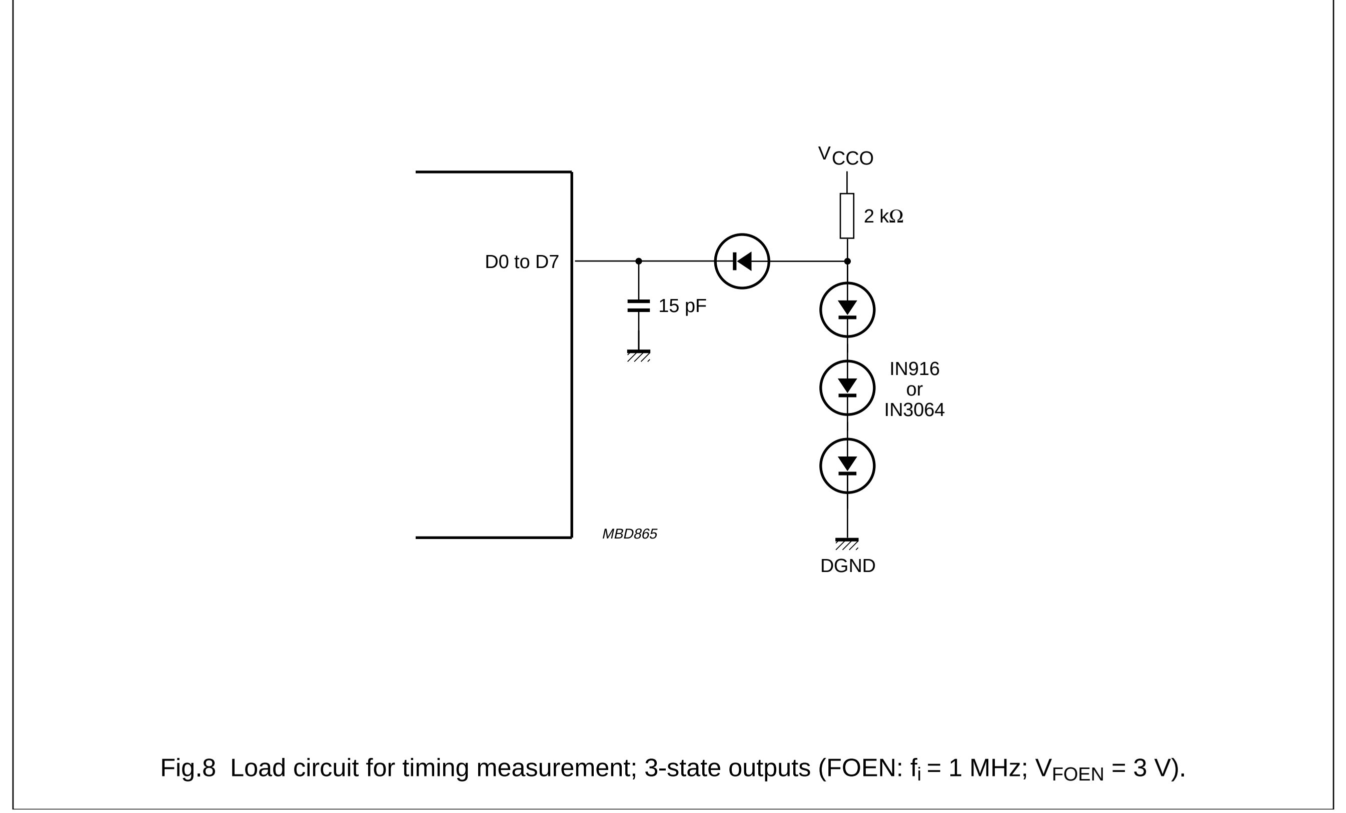
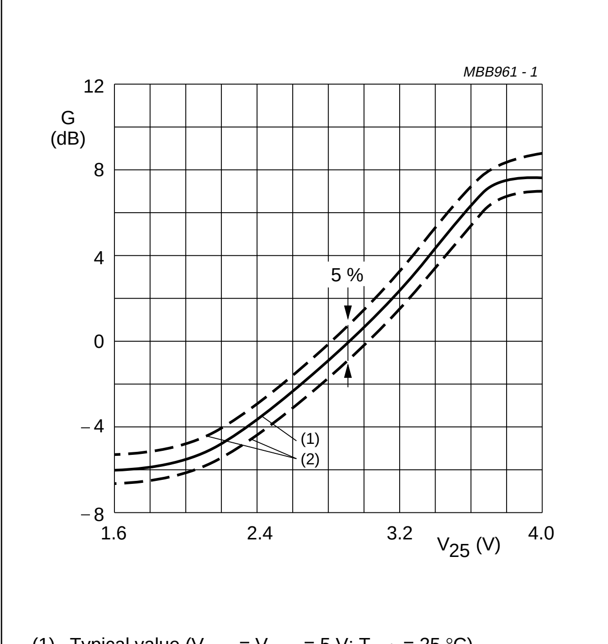


Fig.8 Load circuit for timing measurement; 3-state outputs (FOEN: f_i = 1 MHz; V_{FOEN} = 3 V).



(1) Typical value (V_{CCA} = V_{CCD} = 5 V; T_{amb} = 25 °C).

(2) Minimum and maximum values (temperature and supply).

Fig.9 Typical gain control curve as a function of gain voltage.

INTERNAL PIN CIRCUITRY

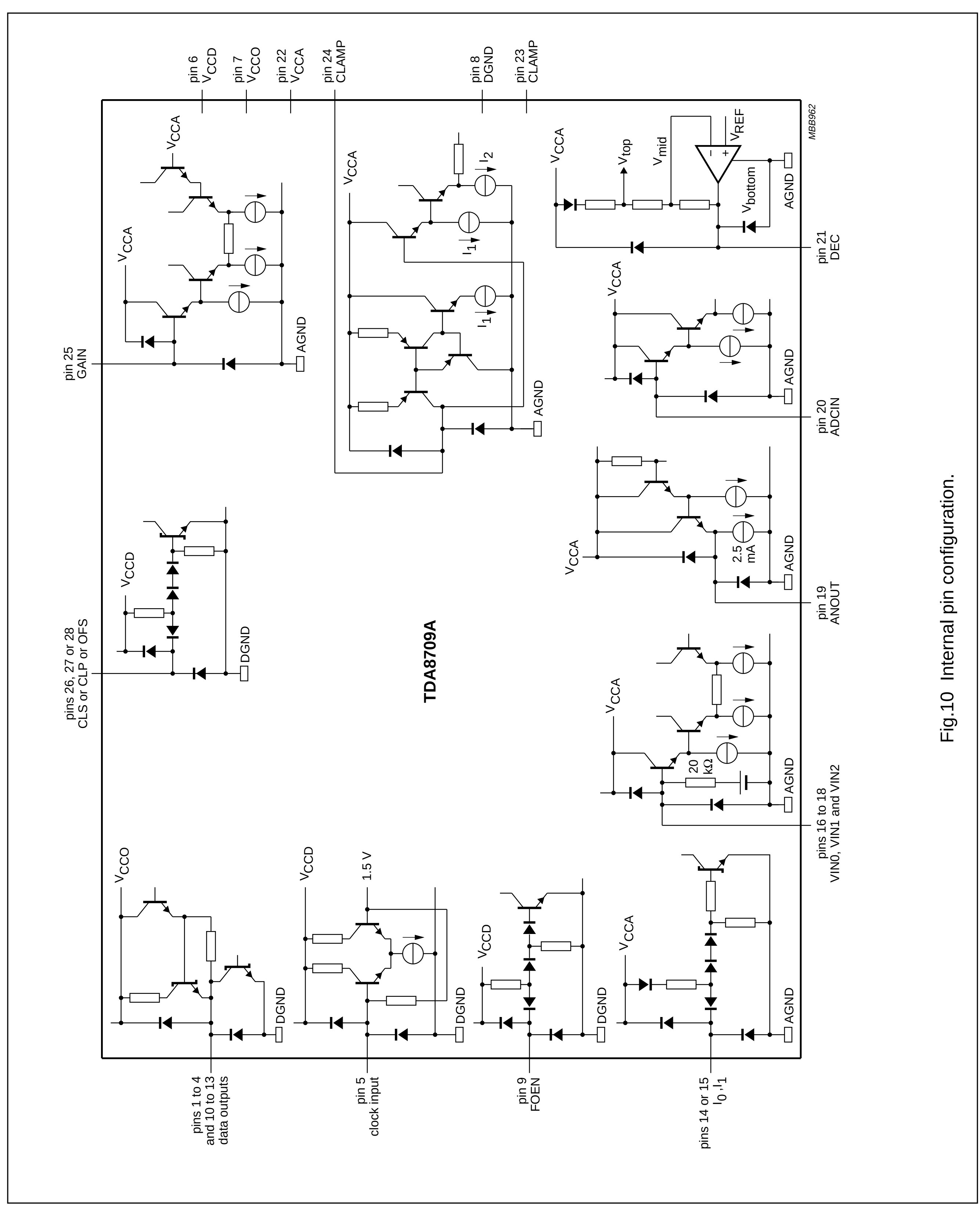
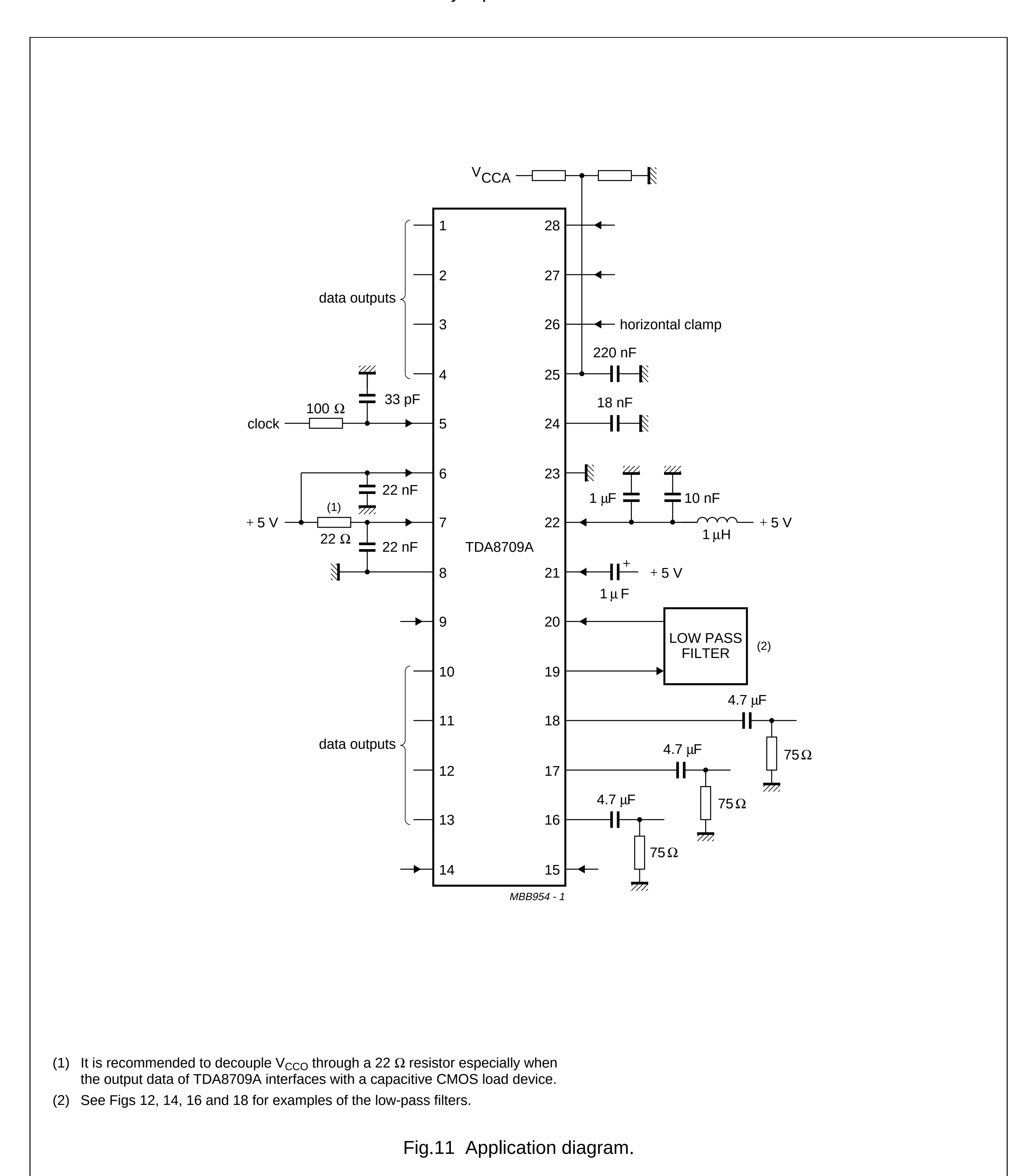


Fig.10 Internal pin configuration.

APPLICATION INFORMATION

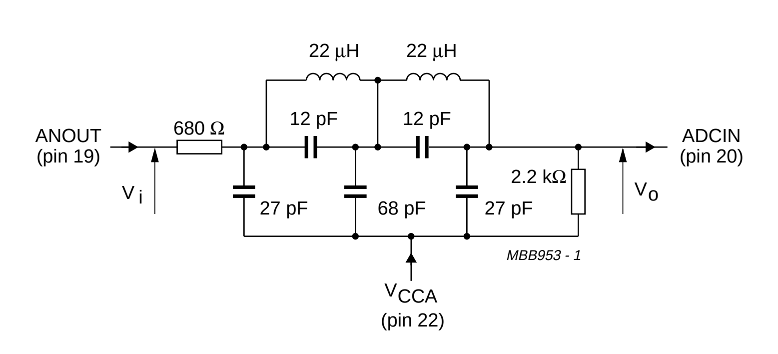
Additional information can be found in the laboratory report of TDA8708A *“FBL/AN9308”*.



(1) It is recommended to decouple V_{CCO} through a 22 Ω resistor especially when the output data of TDA8709A interfaces with a capacitive CMOS load device.

(2) See Figs 12, 14, 16 and 18 for examples of the low-pass filters.

Fig.11 Application diagram.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.12 Example of a low-pass filter for RGB and C signals.

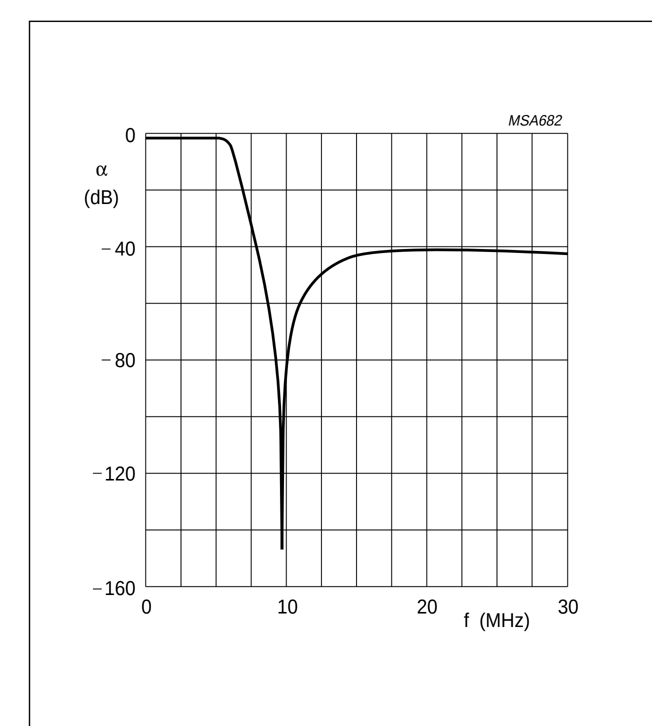
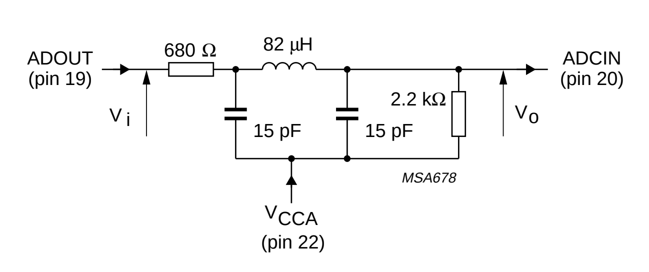


Fig.13 Frequency response for filter shown in Fig.12.

Characteristics of Fig.13

- Order 5; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at −3 dB
- f_{notch} = 9.65 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.14 Example of an economical low-pass filter for RGB and C signals.

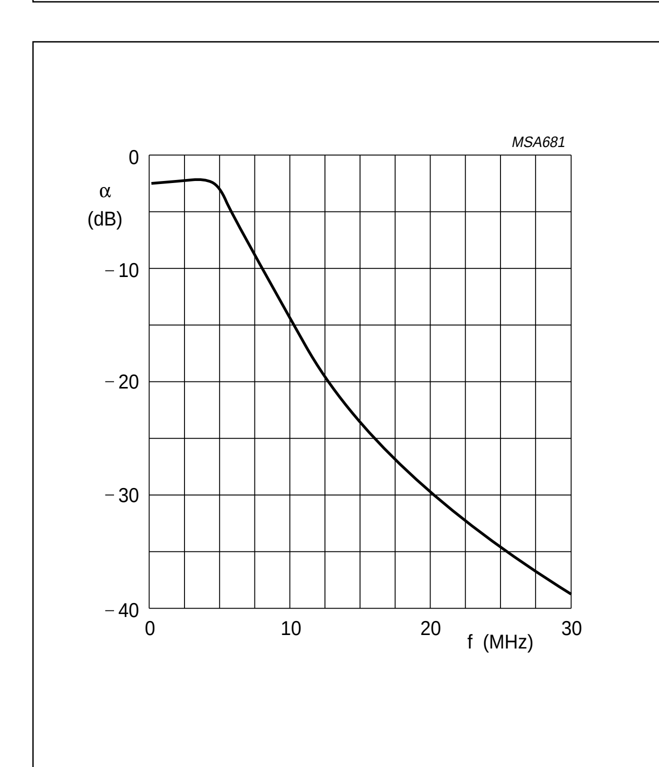
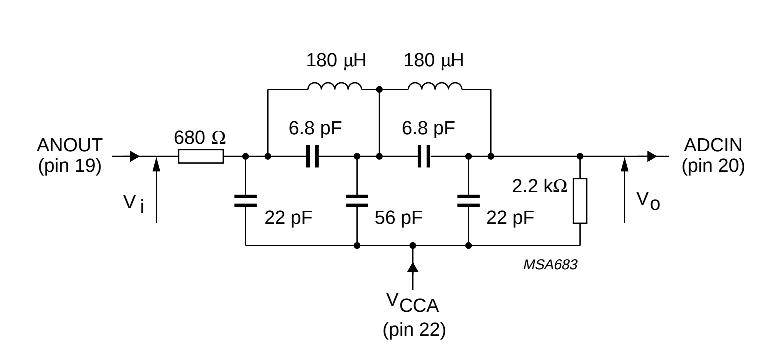


Fig.15 Frequency response for filter shown in Fig.14.

Characteristics of Fig.15

- Order 3; adapted CHEBYSHEV
- Ripple $\rho \leq 0.4$ dB
- f = 6.5 MHz at –3 dB.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.16 Example of a low-pass filter for U and V signals.

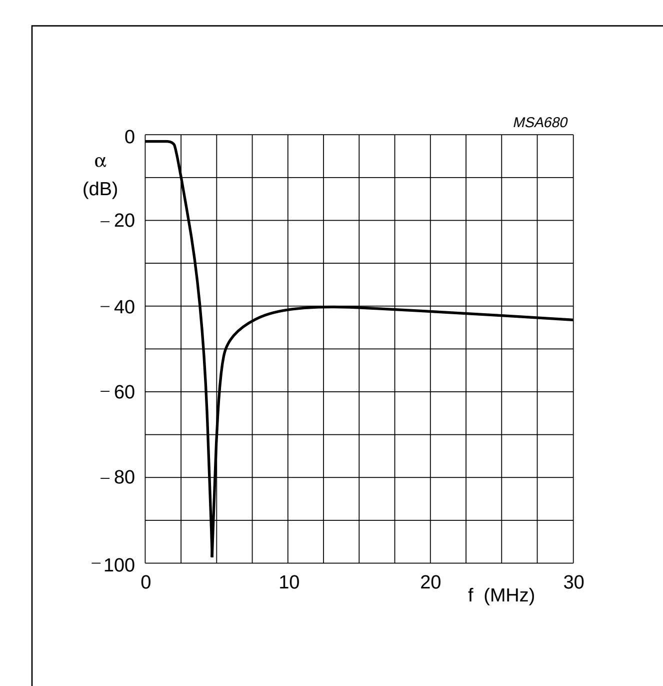
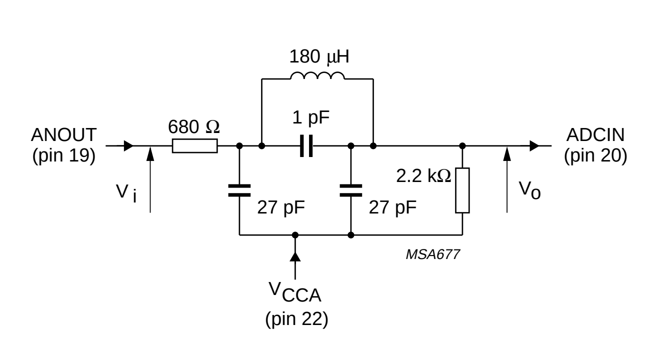


Fig.17 Frequency response for filter shown in Fig.16.

Characteristics of Fig.17

- Order 5; adapted CHEBYSHEV
- Ripple ρ ≤ 0.4 dB
- f = 2.3 MHz at –3 dB
- f_{notch} = 4.5 MHz.



This filter can be adapted to various applications with respect to performance requirements. An input and output impedance of at least 680 Ω and 2.2 kΩ must in any event be applied.

Fig.18 Example of an economical low-pass filter for U and V signals.

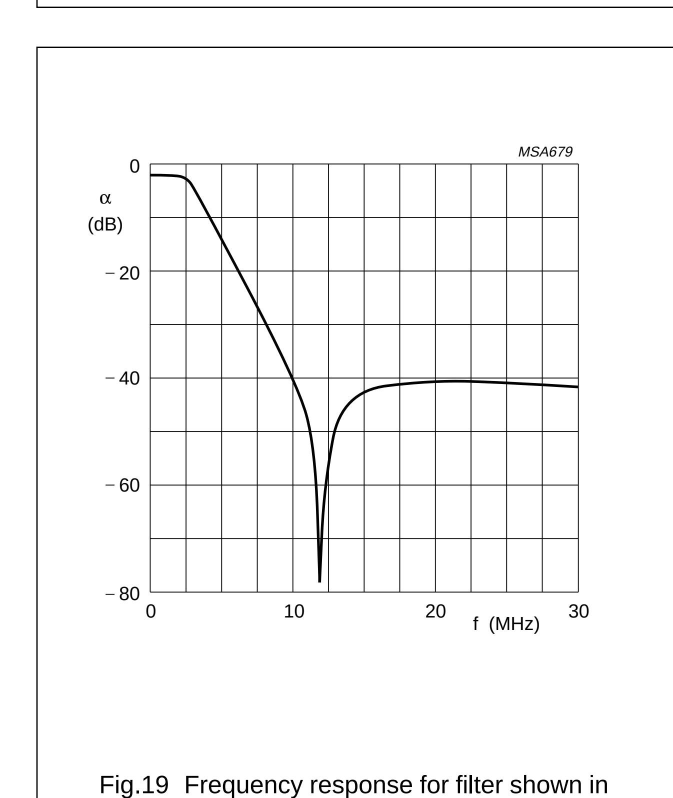


Fig.19 Frequency response for filter shown in Fig.18.

Characteristics of Fig.19

- Order 3; adapted CHEBYSHEV
- Ripple ρ ≤ 0.3 dB
- f = 2.8 MHz at –3 dB
- f_{notch} = 11.9 MHz.

PACKAGE OUTLINES

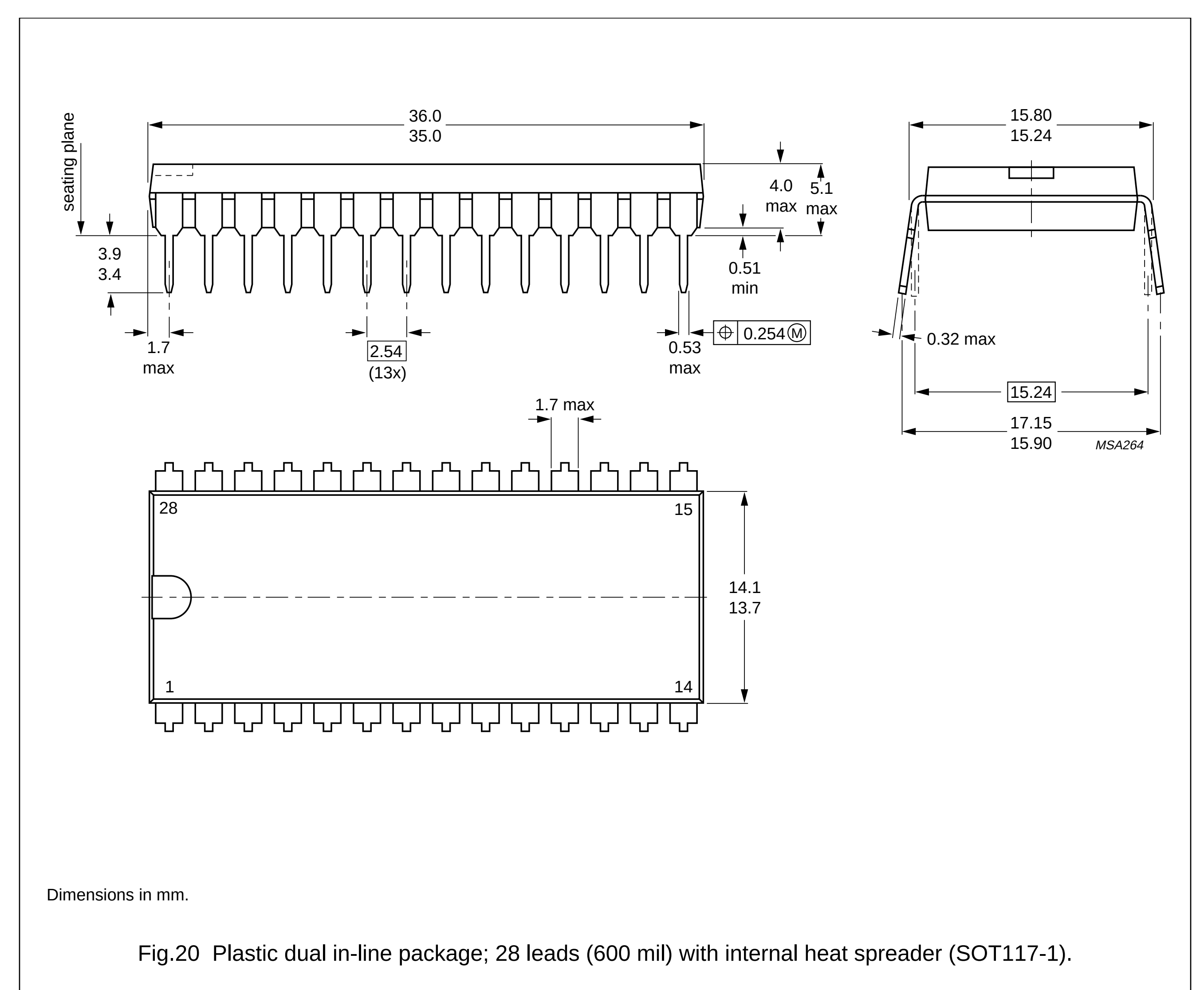


Fig.20 Plastic dual in-line package; 28 leads (600 mil) with internal heat spreader (SOT117-1).

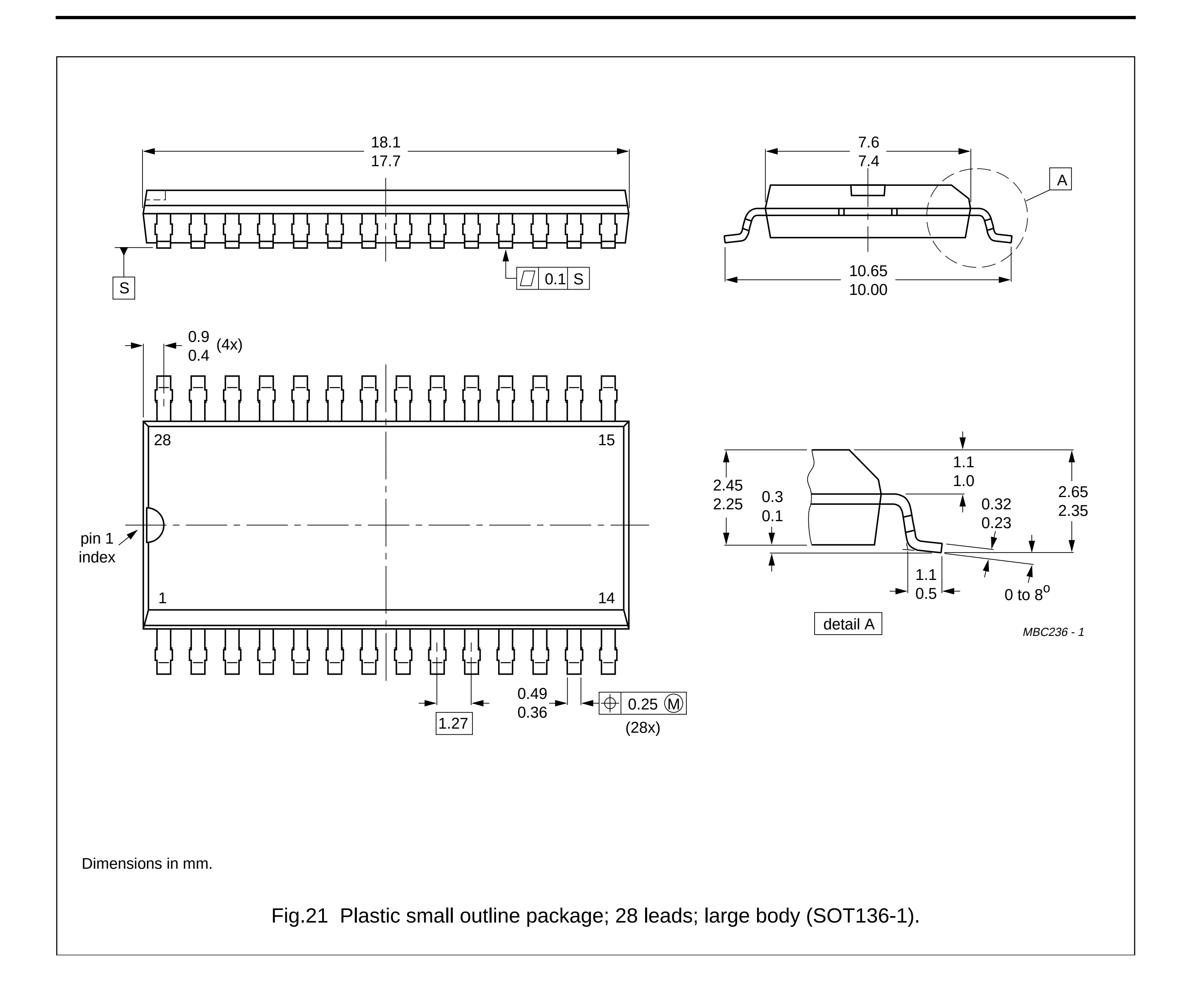


Fig.21 Plastic small outline package; 28 leads; large body (SOT136-1).

SOLDERING

Plastic dual in-line packages

BY DIP OR WAVE

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron below the seating plane (or not more than 2 mm above it). If its temperature is below 300 °C, it must not be in contact for more than 10 s; if between 300 and 400 °C, for not more than 5 s.

Plastic small-outline packages

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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